UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,103,041 B1
APPLICATION NO. : 09/610116
DATED : September 5, 2006
INVENTOR(S) : Speiser et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under Columns 21-56, delete handwritten numbers "41", "42", "43", "44", "45", "46", "47", "48", "49", "50", "51", "52", "53", "54", "55", "56", "57", "58".

In Column 26, below Figure, Line 2, delete "disab" and insert -- disabled) --, therefor.

Signed and Sealed this

Twenty-sixth Day of January, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

APPENDIX

BFS Backplane optimization worksheet

Notes:

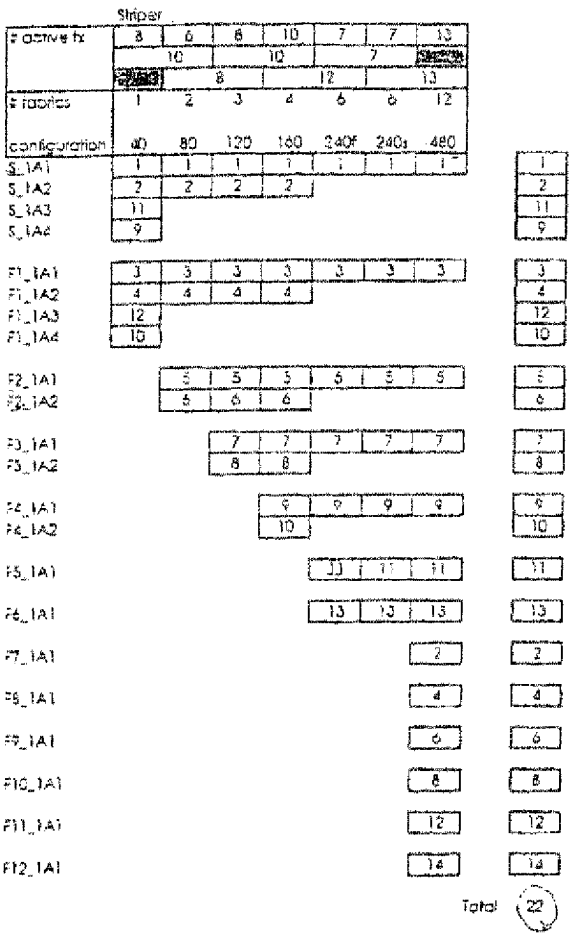
1) Colors are used to represent the use/reuse of serial communication channels.

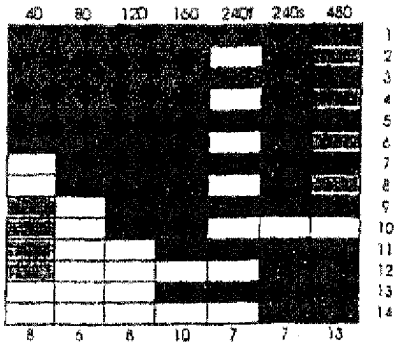
2) Channel assignments are optimized for multiple variables:

- Minimization of I/O. Quad GE transceivers provide 1:2 fanout buffers and 2:1 multiplexers 1:3 fanout or 3:1 fanin requires additional external devices.

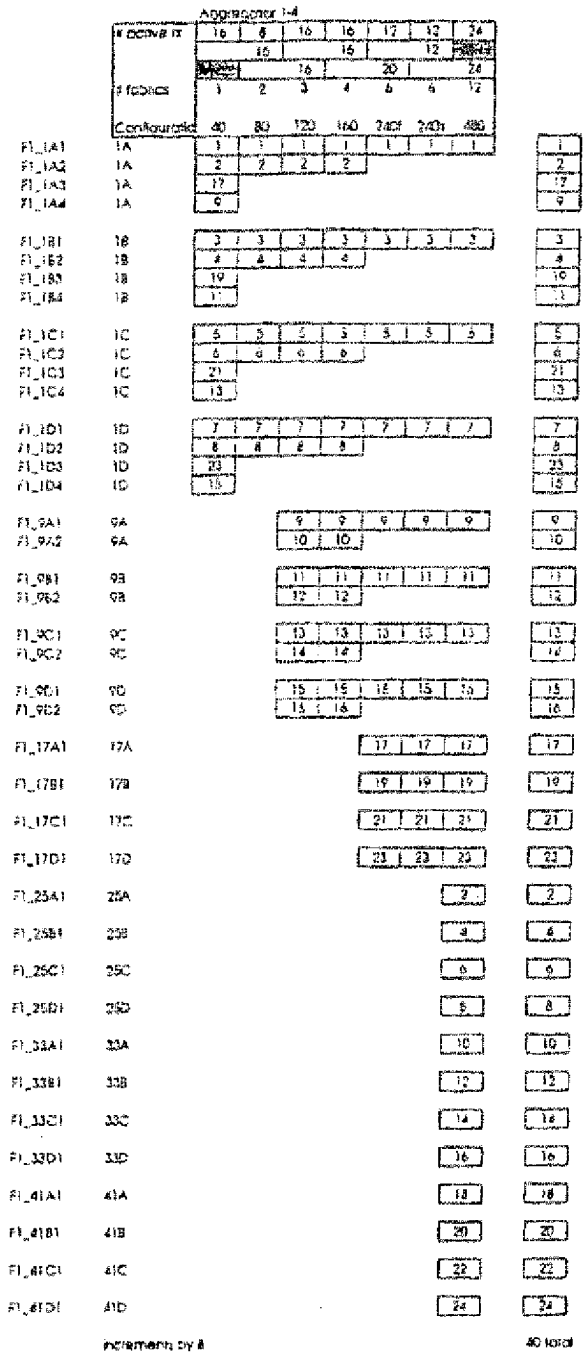
- Partitioning of PCB routing complexity. The ASIC to quad GE buses are ideally straight and interleaved (either with unstriper and aggregator with separator) to simplify the routing of these clocked buses. The serial connections from quad GE transceivers to card edge connector on fabric and blade requires significant unbending (with minimal use of vias) to group signals by common destination on the edge connector. This is required to reduce the complexity of the backplane routing and corresponding layer count.

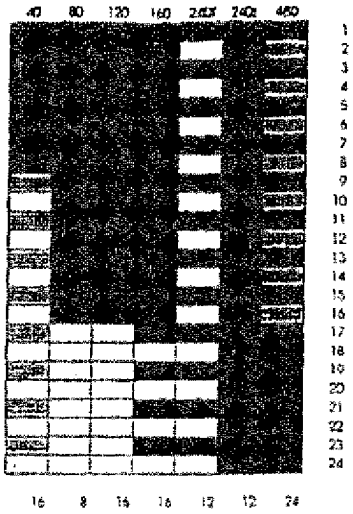
- Maximization of symmetry between ASIC's. This symmetry allows interleaving of buses and reduces the need for external muxs and fanout buffers. It may also reduce the complexity of ASICs by reducing the number of unique mux/demux structures. Consequently, the striper map is a subset of the unstriper map, and both aggregator maps and the separator 5-8 map are derived from the separator 1-4 map.



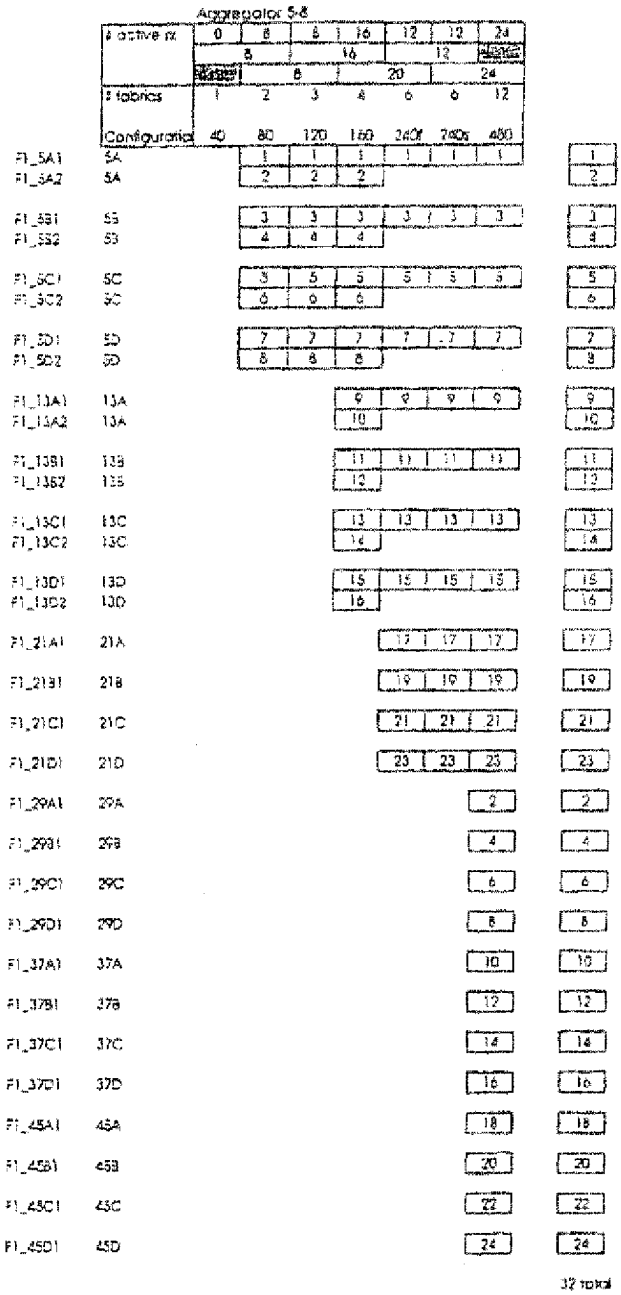


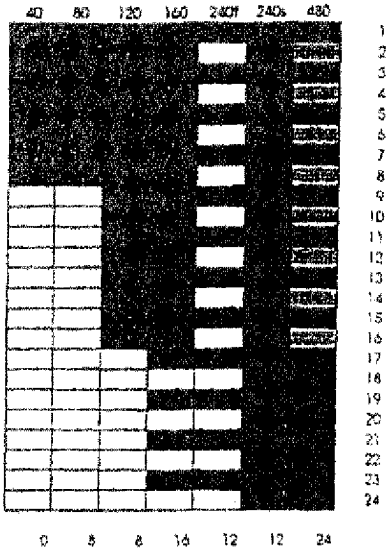
8 internal 1:2 fanout buffers
6 internal 1:1 fanout buffers (one output can be disab



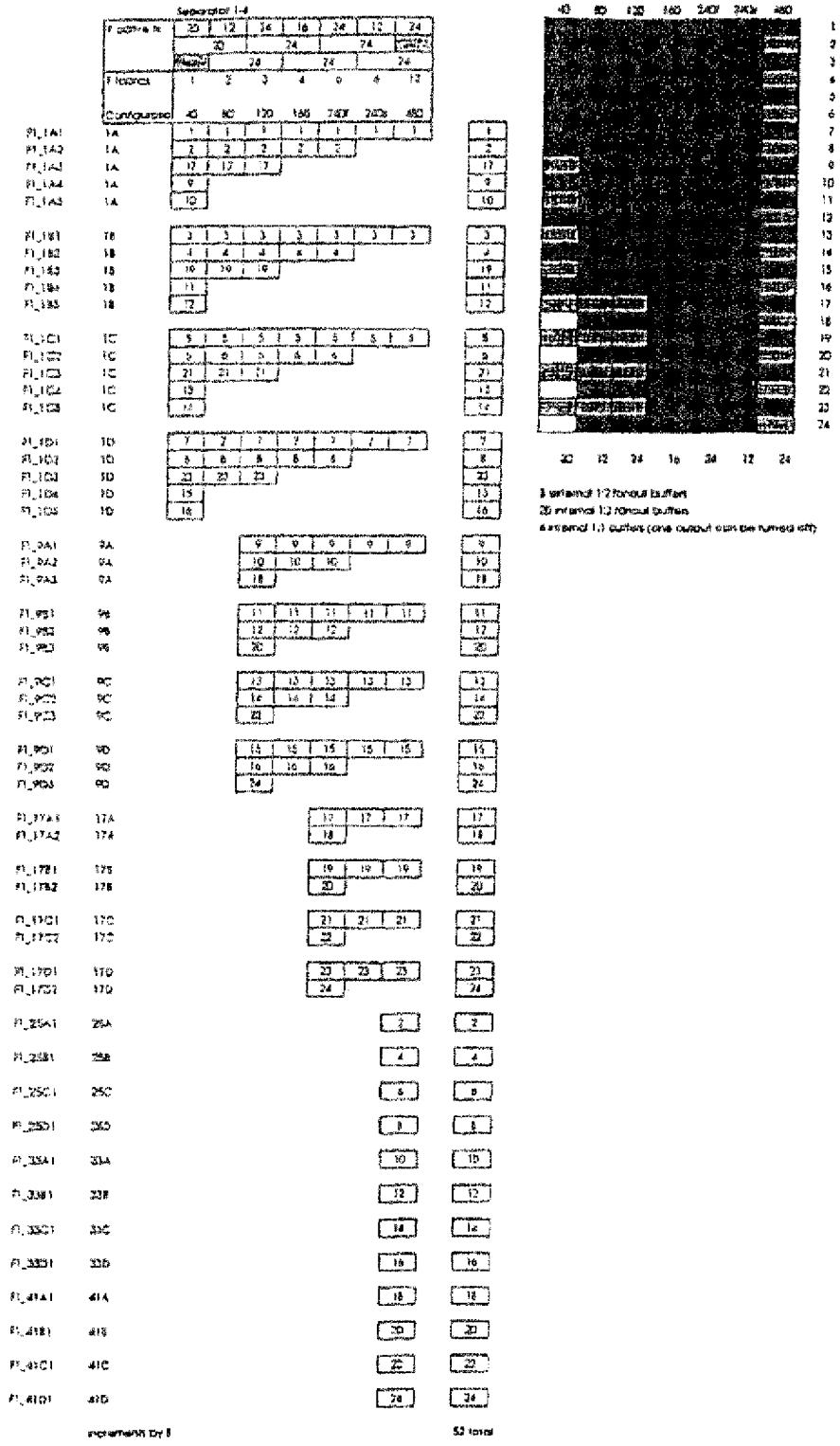


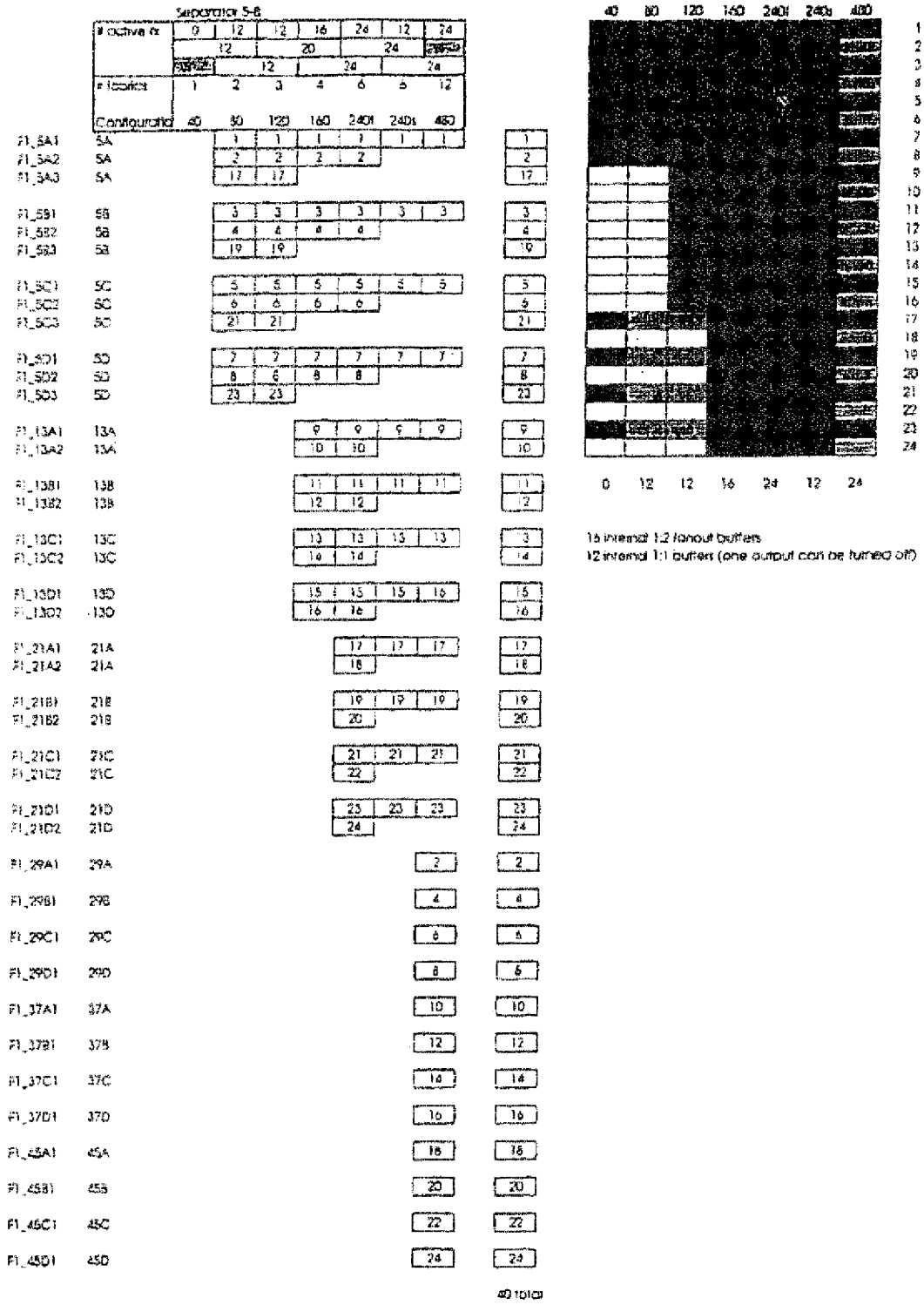
16 internal 2:1 Mux's
8 internal 1:1 buffers (one input can be turned off)

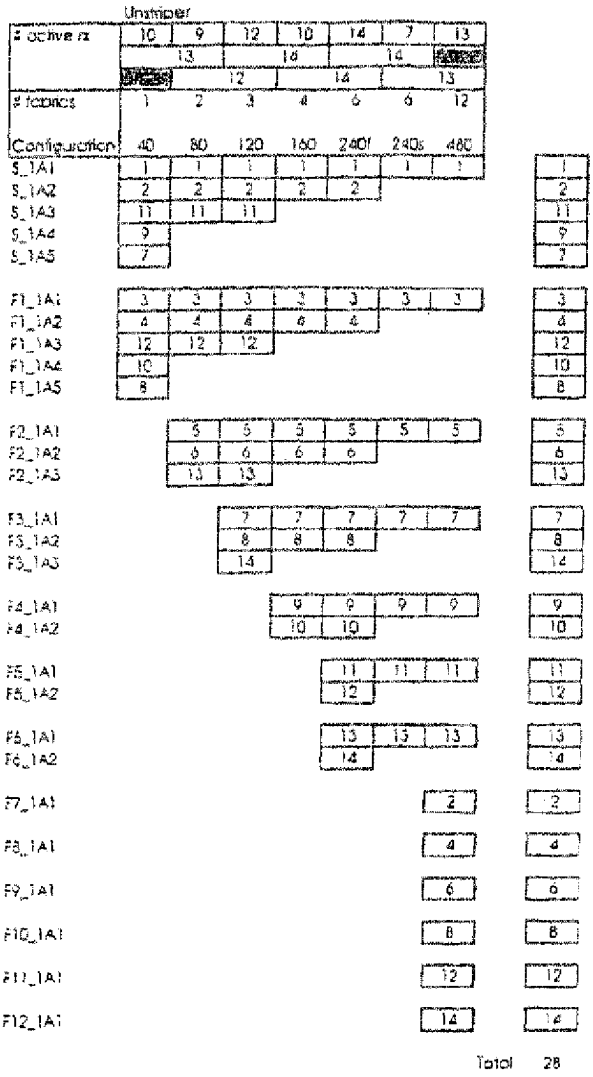


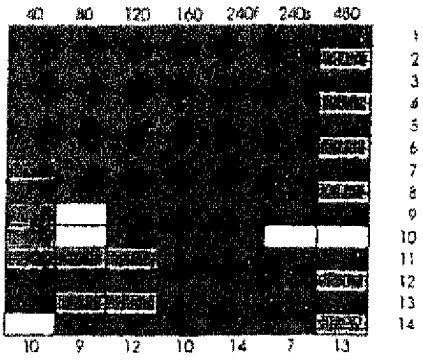


8 internal 2:1 Muxes
16 internal 1:1 buffers (one input can be turned off)




Separator 5-6
active ch
banks
Configuration
40 80 120 160 240i 240s 480
0 12 12 16 24 12 24
16 internal 1:2 fanout buffers
12 internal 1:1 buffers (one output can be turned off)





3 external 2:1 Mux's
11 internal 2:1 Mux's
3 internal 1:1 input buffers (one input can be disabled

BFS ASIC Backplane Connection Map

Revision	Date	Comments
1	11/3/99	First release checked by Spatter
2	11/8/99	Changed 40G assignments for channels 7 and 9; affects the slipper and unslipper only Changed 40, 80, 120G assignments for channels 17-24 to make Separator 1-4 and Separator 5-8 symmetric (Separator 5-8 is now a subset of Separator 1-4)
3	11/30/99	Checked by Spatter and Blanchfield Added control port assignments

Naming convention:

<fabric to blade egress bus format: <fabric>_<blade><channel><lane><polarity>

Fabric slot	Blade slot	Channel	Lane	Polarity
F1-F12,S	1-48	A-D	1-5	P,N

Notes:

1) Map shown for a single instance of each ASIC, e.g. slipper channel A for blade number 1, from an ASIC point of view, all that is significant in this slipper table is the fabric number and the lane number. The topology is the same for each subsequent channel (B-D) blade slot (2-48).

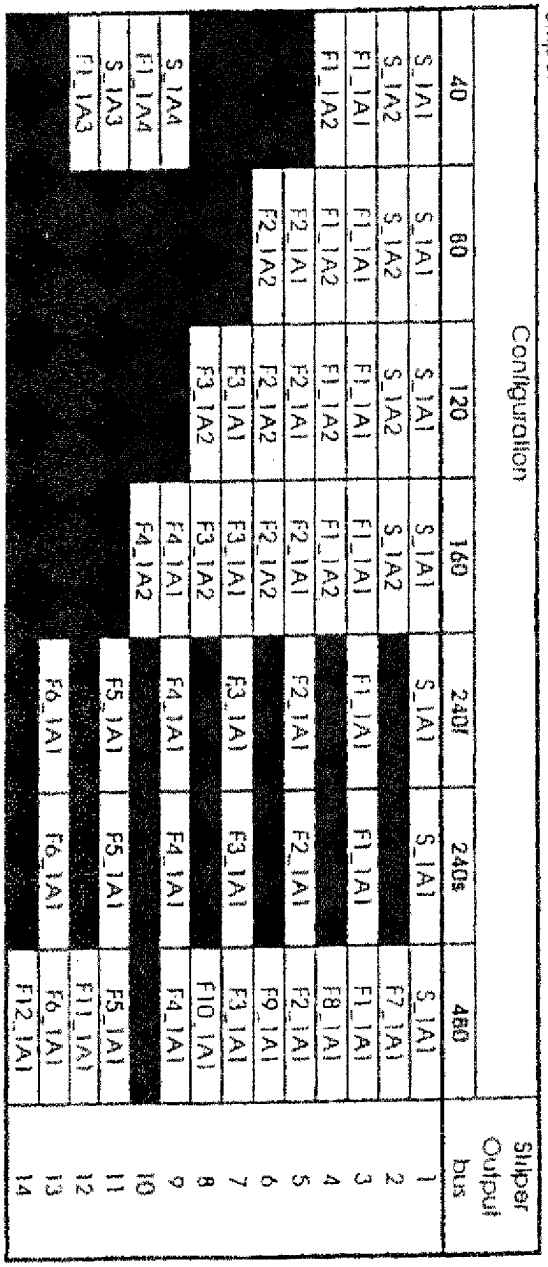
2) Polarity is required to distinguish the two physical wires forming a differential pair. For each table entry (i.e., each logical signal) there are two physical connections For example, logical signal F2_1A3 is really comprised of F2_1A3P and F2_1A3N, which connect fabric 2 to blade 1, unslipper 1, lane 3. Polarity is not shown in the connection maps to make them easier to read.

3) How to use this map: For a given configuration (e.g. with one fabric installed), read down 40 G column) Read down the column to determine the source for data present on an slipper output bus. Each row represents a single slipper output bus.

4) [redacted] = not used in this Configuration

5) To aid in PCB routing and reduce design complexity, there are only two unique connection assignments. The unslipper and the Separator 1-4 maps. The slipper map is a subset of the unslipper map. The separator 5-8 map, the aggregator 1-4 map, and the aggregator 5-8 map are all subsets of the separator 1-4 map.

6) Up to four control ports can supported (see maps for aggregator 9 and separator 9) If not all four control ports are needed, some control port channels can be deleted. For example, if only two 2.5Gbps control ports are needed, control port channels C and D can be deleted


Stripper
Configuration
40
60
120
160
240f
240s
460
Stripper Output bus
S_1A1
S_1A2
F1_1A1
F1_1A2
F2_1A1
F2_1A2
F3_1A1
F3_1A2
F4_1A1
F4_1A2
F5_1A1
F6_1A1
S_1A4
F1_1A4
S_1A3
F1_1A3
F7_1A1
F8_1A1
F9_1A1
F10_1A1
F11_1A1
F12_1A1
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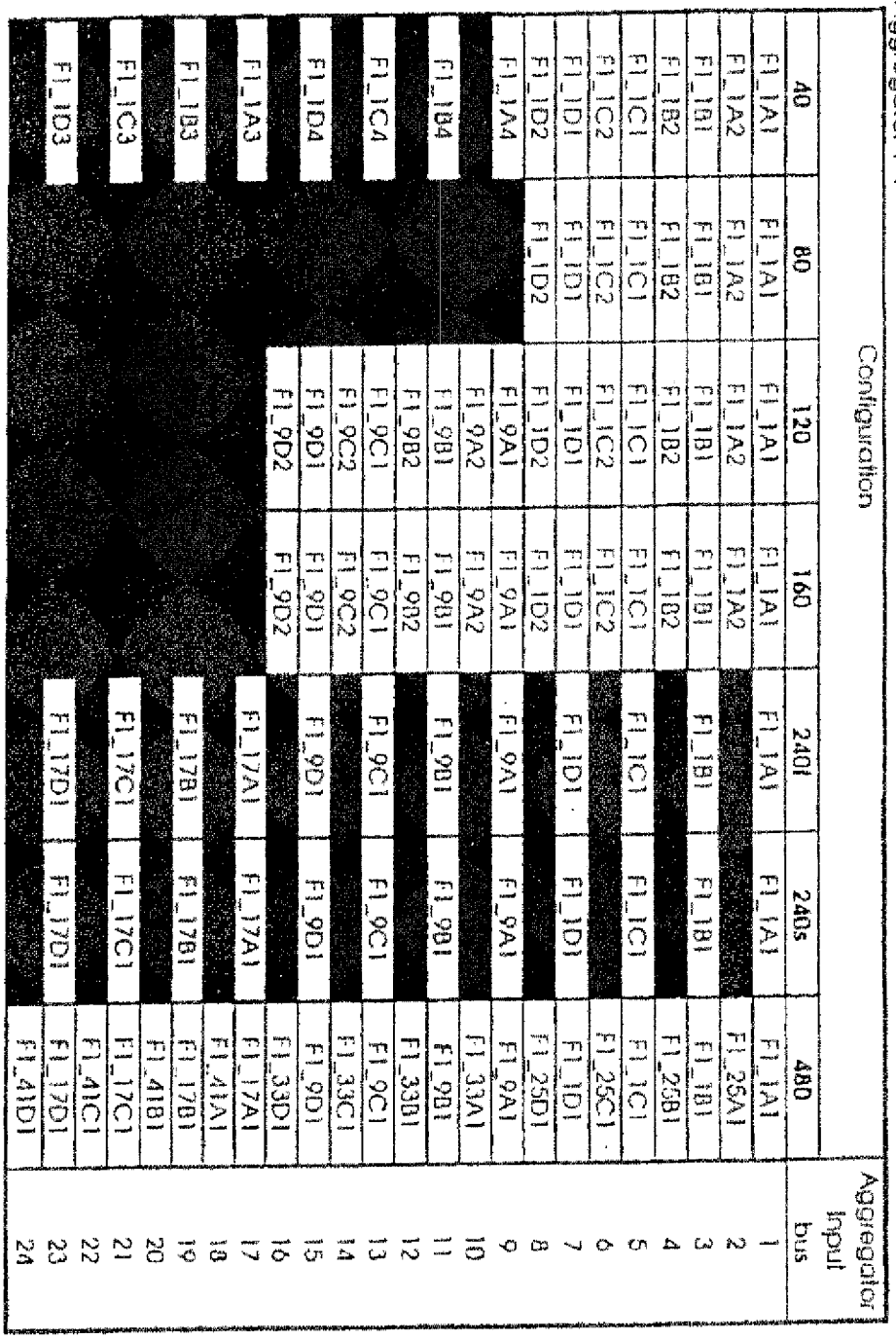
Aggregator 1-4
Configuration
40
80
120
160
240f
240s
480
Aggregator Input bus
F1_1A1
F1_1A2
F1_1B1
F1_1B2
F1_1C1
F1_1C2
F1_1D1
F1_1D2
F1_1A4
F1_1B4
F1_1C4
F1_1D4
F1_1A3
F1_1B3
F1_1C3
F1_1D3
F1_9A1
F1_9A2
F1_9B1
F1_9B2
F1_9C1
F1_9C2
F1_9D1
F1_9D2
F1_17A1
F1_17B1
F1_17C1
F1_17D1
F1_25A1
F1_25B1
F1_25C1
F1_25D1
F1_33A1
F1_33B1
F1_33C1
F1_33D1
F1_41A1
F1_41B1
F1_41C1
F1_41D1
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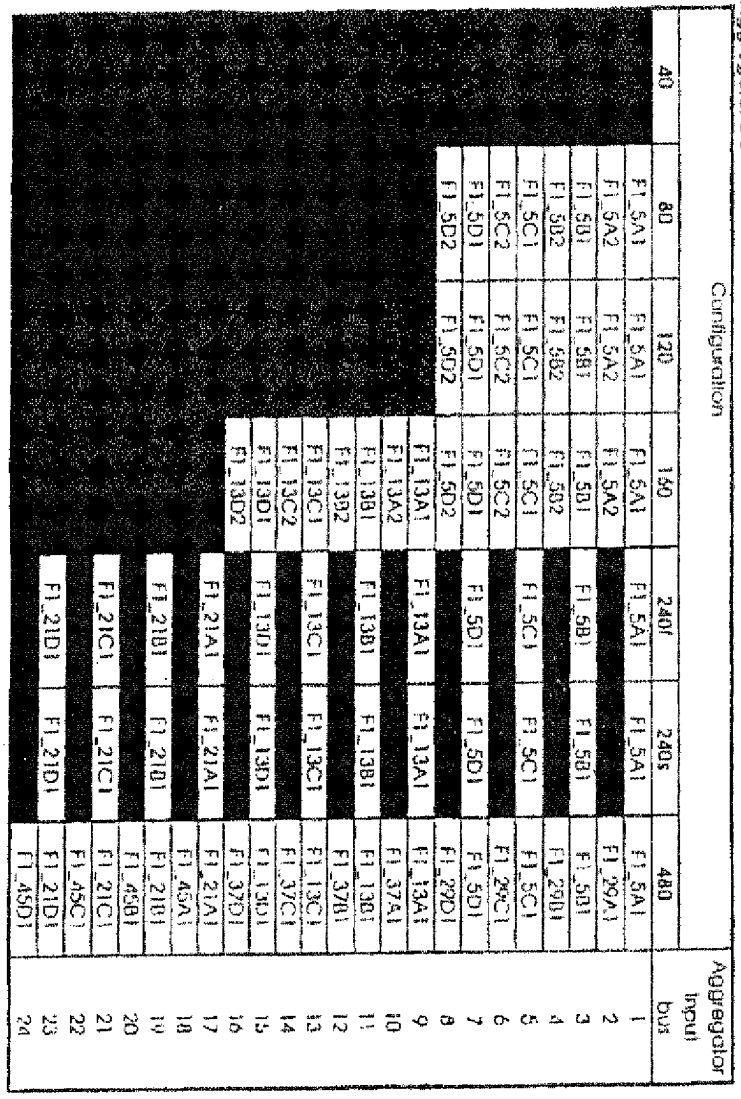
Aggregator 5-8
Configuration
Aggregator Input bus
40
80
120
160
240f
240s
480
F1_5A1
F1_5A2
F1_5B1
F1_5B2
F1_5C1
F1_5C2
F1_5D1
F1_5D2
F1_13A1
F1_13A2
F1_13B1
F1_13B2
F1_13C1
F1_13C2
F1_13D1
F1_13D2
F1_21A1
F1_21B1
F1_21C1
F1_21D1
F1_29A1
F1_29B1
F1_29C1
F1_29D1
F1_37A1
F1_37B1
F1_37C1
F1_37D1
F1_45A1
F1_45B1
F1_45C1
F1_45D1
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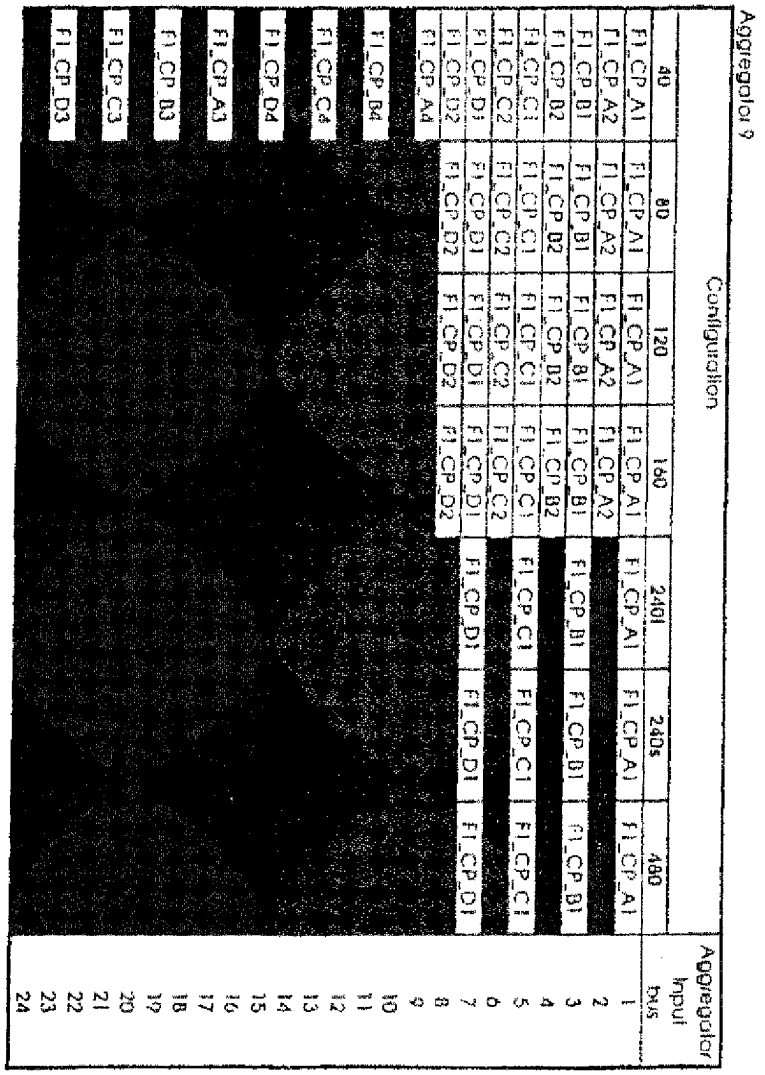
Aggregator 9
Configuration
Aggregator Input bus
40
80
120
160
240i
240s
480
F1_CP_A1
F1_CP_A2
F1_CP_B1
F1_CP_B2
F1_CP_C1
F1_CP_C2
F1_CP_D1
F1_CP_D2
F1_CP_A4
F1_CP_B4
F1_CP_C4
F1_CP_D4
F1_CP_A3
F1_CP_B3
F1_CP_C3
F1_CP_D3
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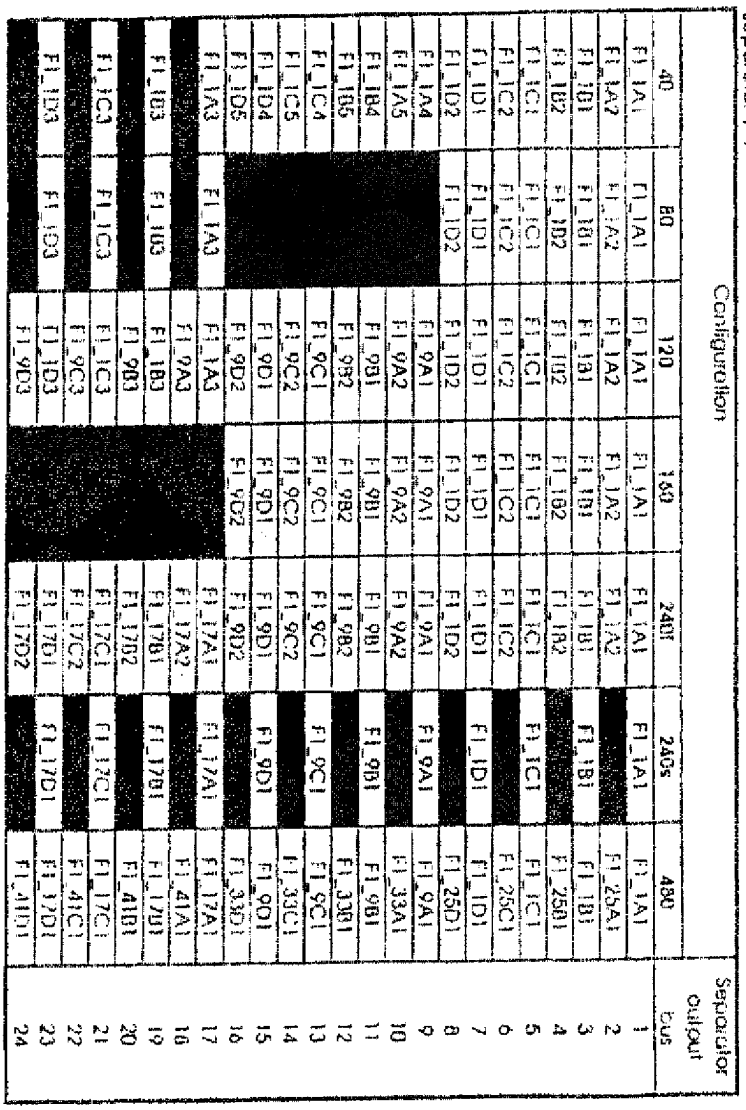
Separator 1-4
Configuration
Separator Output bus
40
80
120
160
240T
240s
480
1
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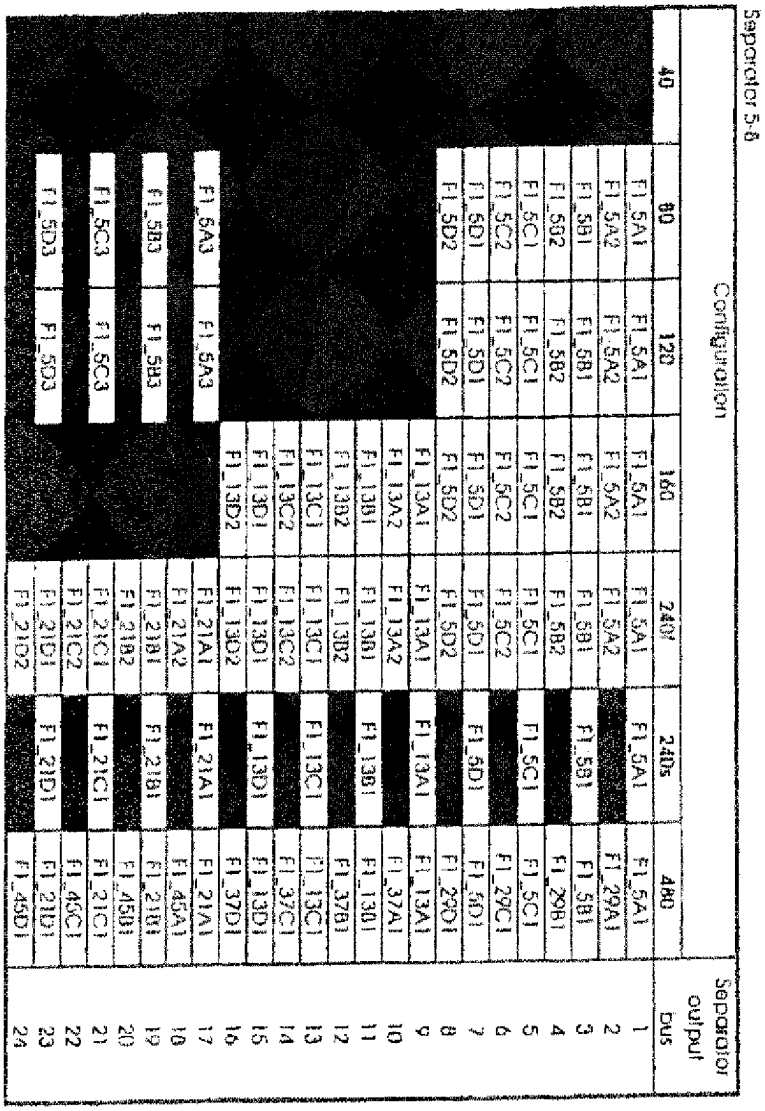
Separator 5-6
Configuration
40
80
120
160
240r
240s
480
Separator output bus
F1_5A1
F1_5A2
F1_5B1
F1_5B2
F1_5C1
F1_5C2
F1_5D1
F1_5D2
F1_5A3
F1_5B3
F1_5C3
F1_5D3
F1_13A1
F1_13A2
F1_13B1
F1_13B2
F1_13C1
F1_13C2
F1_13D1
F1_13D2
F1_21A1
F1_21A2
F1_21B1
F1_21B2
F1_21C1
F1_21C2
F1_21D1
F1_21D2
F1_29A1
F1_29B1
F1_29C1
F1_29D1
F1_37A1
F1_37B1
F1_37C1
F1_37D1
F1_45A1
F1_45B1
F1_45C1
F1_45D1
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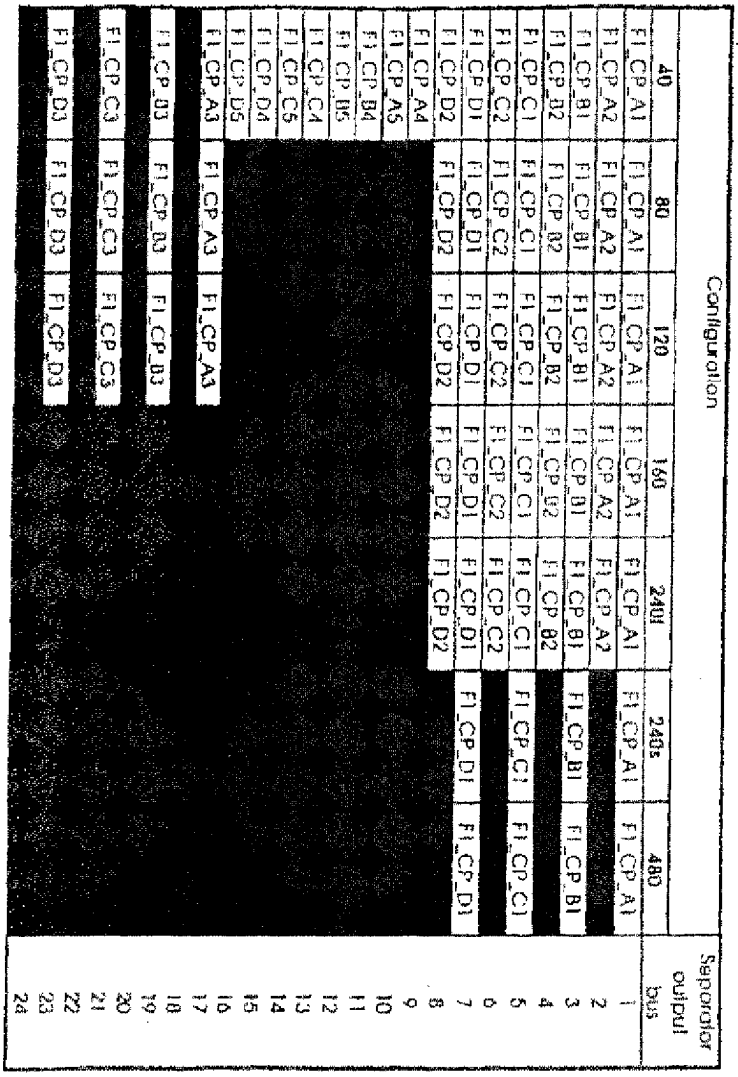
Separator 6
Configuration
40
80
120
160
240i
240s
480
Separator output bus
F1_CP_A1
F1_CP_A2
F1_CP_B1
F1_CP_B2
F1_CP_C1
F1_CP_C2
F1_CP_D1
F1_CP_D2
F1_CP_A3
F1_CP_B3
F1_CP_C3
F1_CP_D3
F1_CP_A4
F1_CP_A5
F1_CP_B4
F1_CP_B5
F1_CP_C4
F1_CP_C5
F1_CP_D4
F1_CP_D5
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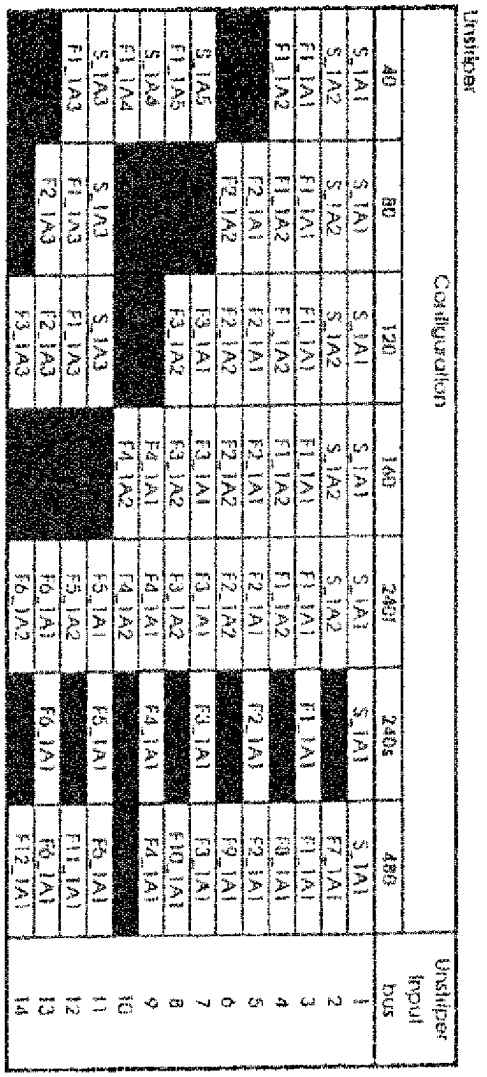
Unstripper
Configuration
Unstripper input bus
40
60
120
140
240i
240s
480
1
2
3
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6
7
8
9
10
11
12
13
14

gigabit signals

Switch size		40	80	120	160	240i	240e	480	<-- gigabits	
number of fabrics		1	2	3	4	6	6	12	<-- does not include spare	
base data bus		12	6	4	3	2	2	1	<-- number of 250MHz data bits from striper to aggregator per OC-48 (4x per port card)	
Calculated										
striper to fabric bus	data in	26	14	10	8	6	6	4	@125MHz to Tx	
	gigabits	3.25	1.75	1.25	1	0.75	0.75	0.5	/8 bits per Tx	
	transmitters	4	2	2	1	1	1	1	round up to unit Tx	
fabric to unstriper bus	data out	52	28	20	16	12	12	8	@125MHz from Rx (w/2x speed-up)	
	gigabits	6.5	3.5	2.5	2	1.5	1.5	1	/8 bits per Rx	
	receivers	7	4	3	2	2	2	1	round up to unit Rx	
Implemented										
striper to fabric bus	transmitters	4	2	2	2	1	1	1	<-- update these numbers to effect input speedup	
fabric to unstriper bus	receivers	5	3	3	2	2	1	1	<-- update these numbers to effect output speedup	
	speedup	1.50	1.87	2.00	2.00	2.00	1.00	2.00	speed-up assumes always use 4 RW bits in egress direction	
Configs		40/80	80/120	120/160	160/240i	240i/240e	240e/480		required simultaneous modes	
Port Card										
striper	active Tx	10	8	10	12	7	13	13	max active Tx	number of serializers per striper
unstriper	active Rx	13	12	14	14	14	13	14	max active Rx	number of deserializers per unstriper
unique streams								56		number of tranceivers per port card
								14		number of quad tranceivers per port card
total streams										
striper	Tx increment	10	2	2	2	0	6	22	total Tx	number of gigabit backplane connections per striper
unstriper	Rx increment	13	3	2	4	0	5	24	total Rx	number of gigabit backplane connections per unstriper
								200		number of gigabit backplane connections per port card
								400		number of pins per port card
Fabric										
Agg1-4	active Rx	16	16	16	20	12	24	24	max active Rx	number of deserializers per odd aggregator
Agg5-8	active Rx	8	8	16	20	12	24	24	max active Rx	number of deserializers per even aggregator
Sep1-4	active Tx	20	24	24	24	24	24	24	max active Tx	number of serializers per odd separator
Sep5-8	active Tx	12	12	20	24	24	24	24	max active Tx	number of serializers per even separator
unique streams								192		number of trancievers per fabric
								48		number of quad tranceivers per fabric
total streams										
Agg1-4	Rx increment	16	8	0	4	0	12	40	total Rx	number of gigabit backplane connections per odd aggregator
Agg5-8	Rx increment	8	0	8	4	0	12	32	total Rx	number of gigabit backplane connections per even aggregator
Sep1-4	Tx increment	20	12	0	8	0	12	52	total Tx	number of gigabit backplane connections per odd separator
Sep5-8	Tx increment	12	0	8	8	0	12	40	total Tx	number of gigabit backplane connections per even separator
								656		number of gigabit backplane connections per fabric
								1312		number of pins per fabric